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A comparative study on the electrical characteristics of Au/n-Si structures with anatase and rutile phase TiO_2 interfacial insulator layer

A. Bengi*, U. Aydemir, Ş. Altındal, Y. Özen, S. Özçelik

Department of Physics, Faculty of Arts and Sciences, Gazi University, 06500, Ankara, Turkey

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ABSTRACT

TiO_2 thin films were deposited on polycrystalline n-type Si substrate using DC magnetron sputtering system. To improve the crystal quality, thermal annealing (TA) process was done at 700 °C and 900 °C. The effect of TA on the structural properties was investigated using high resolution X-ray diffraction (HRXRD). It was observed that the phase transition from amorphous phase to anatase and rutile phases occurs at 700 °C and 900 °C, respectively. Au/TiO_2/n-Si structures were also fabricated for the investigation of TA on the main electrical parameters, such as ideality factor (n), barrier height (Φ_B), series resistance (R_s), shunt resistance (R_{sh}) and interface states (N_{ss}). The current–voltage (I–V) and capacitance–voltage (C–V) characteristics have been investigated at room temperature and results have been compared with each other. The electrical characteristics showed that TA strongly affects the main electrical parameters. The rectifying ratio of Au/n-Si structures with anatase phase TiO_2 was to be 140 while the rutile phase was to be 8864. The leakage current was also found to be very sensitive to the annealing temperature, and also the magnitude of the leakage current for rutile phase is 15 times lower than the anatase phase's. In addition, the energy distribution profile of N_{ss} of the structures was obtained from the forward bias I–V data by taking the bias dependence of the effective barrier height (Φ_e) into account. For both of the samples, the value of N_{ss} decreases with TA. Similarly, the values of R_s and R_{sh} of the structures obtained from the forward bias I–V data were found as 209 Ω and 42 kΩ for the anatase and 59 Ω and 598 kΩ for the rutile phase. These results show that the performance of the Au/TiO_2/n-Si structure improved with thermal annealing.

1. Introduction

Alternative high-k materials such as Si_3N_4, HfO_2, ZnO, ZrO_2 TiO_2, Al_2O_3 for SiO_2 have recently attracted great attention for its application as an interfacial insulator layer at metal/semiconductor (M/S) interface in the semiconductor devices such as metal-insulator/oxide-semiconductor (MIS or MOS) [1–13]. SiO_2 has a poor interface due to high leakage current, high temperature dispersion and high defect trapped charges. Therefore, the fundamental requirement is using high k-dielectrics materials. In addition to high dielectric constant and band offers, low density of interface states and low leakage current [6–13]. Among these high-k materials, bulk TiO_2 is a potential candidate because of having different phases with extraordinarily high dielectric constant. There are three types of bulk crystal structure in TiO_2: (1) anatase, (2) rutile and (3) brookite type with 3.20 eV, 3.02 eV and 2.96 eV energy band gaps, respectively. Among them the brookite phase is an unstable rhombic structure. The most common phases are anatase and rutile phases whose dielectric constants are 48 and 89, respectively [1]. The anatase phase is normally formed around 600 °C, while transformation to rutile phase occurs around 800 °C [1,14–17]. In addition, the anatase phase has an indirect band gap, whereas the rutile phase has a direct band gap [15,16]. The rutile phase in particular has its potential applications in catalysis, electrochromism, high-speed memory devices, paints etc. [3,4].

There are lots of TiO_2 thin film growth techniques such as chemical vapor deposition [18], electron beam evaporation [19], thermal or anodic oxidation [8,20], sol–gel method [21,22], plasma-enhanced chemical vapor deposition [23], and DC reactive magnetron sputtering methods [24,25]. Among these methods, DC reactive magnetron sputtering method is much more preferable since it is easier to control and this method makes the fabrication of insulator films with reproducible and desired properties possible. The performance and reliability of TiO_2 based devices particularly depends on the formation of TiO_2 layer at M/S interface, annealing temperature, density of interface states (N_{ss}) at Si/TiO_2 interface, series resistance (R_s) of devices, and inhomogeneities of the Schottky barrier formation at M/S interface [18–22]. Kadoshima et al. [26] showed that the SiO_2 formation is inevitable during thermal annealing of TiO_2 and it decreases leakage current. Also, Lee et al.

* Corresponding author.
E-mail address: aylinbengi@gmail.com (A. Bengi).

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[17] suggested that the decrease of leakage current was related to the growth of interfacial layer and the reduction of oxygen vacancy.

In general, the forward bias *I–V* characteristics of MIS structure are linear on a semi-logarithmic scale at intermediate bias voltage but deviate considerably from linearity due to the effect of R_s and N_{ss} when the applied voltage is sufficiently large ($V \geq 1$ V). Usually, interface states can be divided into two groups in the view of interfacial insulator layer thickness (δ). One of these groups ($\delta \leq 30$ Å) communicates most rapidly with the metal, while the other group ($\delta \geq 30$ Å) communicates most rapidly with the semiconductor [27,28]. The relation among the semiconductor and the value of ideality factor (n), increases as the insulator layer thickness increases. The values of R_s and N_{ss} can also affect the *C–V* characteristics of devices, by causing a bending of *C–V* plots in the accumulation region.

In this study, the main electrical parameters of Au/TiO_2/n-Si structures with anatase and rutile phase TiO_2 interfacial insulator layer such as ideality factor, leakage current, barrier height, series resistance, shunt resistance and density of interface states have been investigated at room temperature using forward and reverse bias *I–V* and *C–V* measurements. The purpose of this study is to make a comparison of the main electrical parameters of Au/n-Si structures with anatase and rutile phase TiO_2 thin films in terms of N_{ss} and R_s to determine the most suitable one for device applications. In addition, the energy distribution profile of N_{ss} of the Au/TiO_2/n-Si (MIS) structures were obtained from the forward bias *I–V* characteristics by taking both the bias dependence of the effective barrier height and R_s for these kind of films into account and the obtained results were compared with each other.

2. Experimental details

Au/TiO_2/n-Si structures were fabricated on a 2″ diameter with (1 0 0) orientation, 350 μm thickness, 0.01 Ω cm resistivity and phosphorus doped (n-type) polycrystalline Si substrate. TiO_2 thin films with 1500 Å thickness were deposited on n-Si substrate using DC magnetron sputtering system. Prior to the deposition of the TiO_2 thin film, the Si substrate was cleaned using $CHClCCl_2$, CH_3COCH_3, and CH_3OH organic solvents, respectively. After the cleaning step, the Si substrate was etched in a sequence of H_2SO_4 and H_2O_2 20% HF, a solution of $6HNO_3$:1HF:35H_2O, 20% HF and finally rinsed in de-ionized water (resistivity of 18 MΩ cm). Latter to cleaning and etching steps, the Si substrate was mounted on the stainless steel optically heated sputtering holder and loaded in the DC magnetron sputtering system. Before the TiO_2 deposition, Si substrates were heated up to 400 °C in 10^{-8} mbar vacuum and sputter cleaned in pure argon ambient to ensure the removal of any residual organics. After the preparation of the substrate for the deposition of TiO_2 thin film, the Si substrate was transferred into the deposition chamber. TiO_2 thin film was deposited using high purity (99.999%) Ti target, under specific Ar + O_2 reactive gas mixture (Ar/O_2 = 90/10 sccm) controlled with mass flow controllers. For the deposition, the substrate temperature and the pressure was set to 200 °C and 4.2×10^{-3} mbar, respectively and kept constant during the whole deposition.

The deposited TiO_2/n-Si sample was cut into three pieces and thermal annealing process in air for 4 h at 700 °C and 900 °C were held to improve the film quality. The structural changes due to temperature dependent phase transitions from amorphous phase to anatase or rutile phases were carried out using high resolution X-ray diffraction (HRXRD). According to the HRXRD measurements, the as-deposited sample shows the amorphous structure while the samples annealed at 700 °C and 900 °C shows anatase and rutile phases, respectively.

After the structural characterization, the electrical characterization was done to compare the main electrical parameters such as ideality factor, leakage current, barrier height, series resistance and density of interface states. For the electrical characterization, firstly the ohmic and rectifier contacts were formed using thermal evaporation system. The ohmic back contacts were formed by deposition of high purity Au (99.999%) at 450 °C, under 10^{-7} mbar vacuum and the sample was annealed at 400 °C to achieve good ohmic contact behavior. Then, the sample was also tested to see whether or not it has a good ohmic contact behavior. After then, dot shaped rectifier front contacts with 2 mm diameter and 1000 Å thickness were formed by deposition of high purity Au (99.999%) at 70 °C. After the completion of the fabrication of Au/TiO_2/n-Si structures, current–voltage (*I–V*) measurements were performed using Keithley 2400 source-meter and capacitance–voltage (*C–V*) measurements were performed using HP 4192 A LF impedance analyzer (5 Hz to 13 MHz) at 1 MHz. The whole electrical measurements were made at room temperature and performed using micro computer through an IEEE-488 AC/DC converter card.

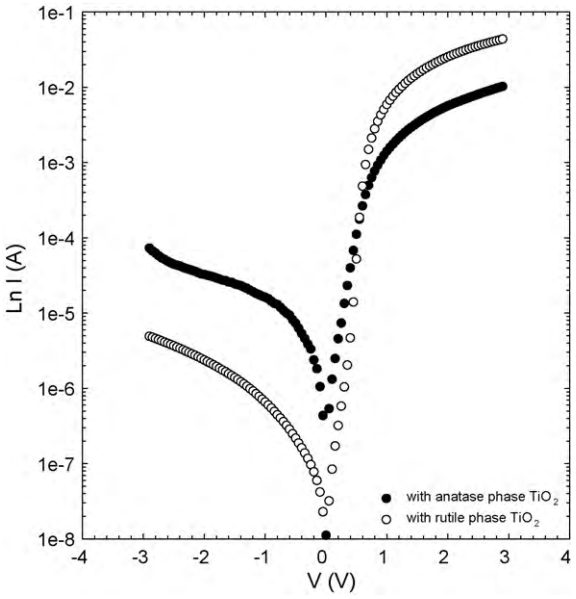

Fig. 1. The semi-logarithmic forward and reverse bias ln *I–V* plots of the Au/n-Si structures with anatase and rutile phase TiO_2 interfacial insulator layer.

3. Results and discussion

Fig. 1 shows the semi-logarithmic forward and reverse bias ln *I–V* plots of the Au/n-Si structures with anatase and rutile phase TiO_2 interfacial insulator layer. As can be seen from the Fig. 1, the rectifying ratio of Au/n-Si structure with anatase phase TiO_2 was found as 140 while the one with rutile phase was found as 8864. However, it deviates considerably from linearity at high forward bias voltages due to the effects of some factors such as series resistance (R_s), interfacial insulator layer and interface states (N_{ss}), etc. In addition, the current rises slowly with the applied reverse bias and does not show any effect of saturation for both types of Au/n-Si structures. This non-saturating behavior of reverse current may be explained in terms of the image force lowering of Schottky barrier height [28] and the presence of the interfacial insulator layer at metal–semiconductor interface [28–43]. The leakage current was also found to be very sensitive to the annealing temperature and the magnitude of the leakage current for rutile phase is 15 times lower than the anatase phase's. These results can be attributed to the reduction of N_{ss} and R_s with thermal annealing in air and as a result the *I–V* characteristics were improved by thermal annealing affect.

For a metal-semiconductor (MS) or metal-insulator-semiconductor (MIS) structures, the relation between current and applied forward voltage ($V > 3kT/q$) can be expressed as [27–29],

$$I = AA^*T^2 \exp\left(-\frac{q\Phi_{Bo}}{kT}\right)\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \quad (1)$$

where V is the applied bias voltage, q is the electronic charge, n is the ideality factor, k is the Boltzmann constant and T is the absolute temperature in Kelvin. The reverse saturation current I_o is extracted from the straight-line intercept of ln *I–V* plot at zero-bias and given by,

$$I_o = AA^*T^2 \exp\left(-\frac{q\Phi_{Bo}}{kT}\right) \quad (2)$$

where A is the rectifier contact area, A^* is the effective Richardson constant (112 A/cm^2 K^2 for n-type Si) and Φ_{Bo} is the apparent barrier height at zero-bias, which can be obtained from Eq. (2). The ideality factor, n, is introduced to take the deviation of the experi-

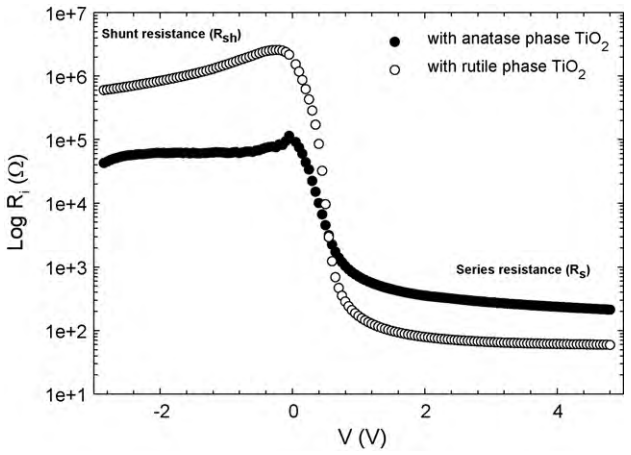

Fig. 2. The structure resistance of Au/n-Si structures with anatase and rutile phase TiO_2.

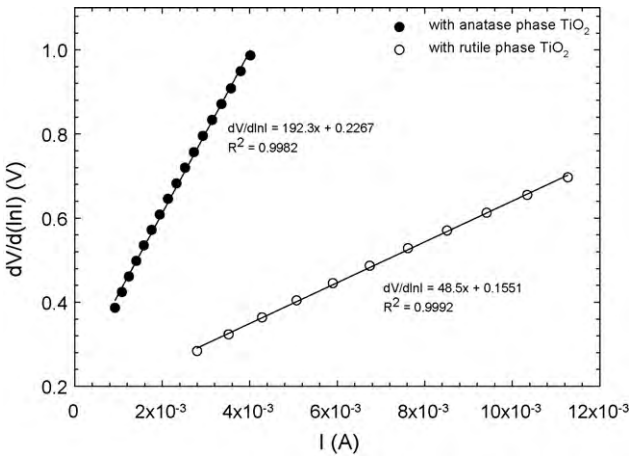

Fig. 3. The $dV/d(\ln I) - I$ characteristics of the Au/n-Si structures with anatase and rutile phase TiO_2 interfacial insulator layer.

mental I–V data from the ideal TE theory into account. From Eq. (1), the value of n is calculated from the slope of the linear region of the forward bias ln I–V plot and can be written as,

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right) \tag{3}$$

The experimental values of Φ_{Bo} and n of Au/n-Si structures with anatase and rutile phase TiO_2 were calculated from Eq. (2) and Eq. (3) as 3.636 eV and 0.603 eV and 2.884 eV and 0.686 eV, respectively. There happens an increase in Φ_{Bo} and a decrease in the n as the annealing temperature increases. It is clear that the ideality factors of the structures are considerably larger than unity. These high values of n show that the device behaves as MIS structure rather than MS structure. The high values of n can be also attributed to existence of an insulator layer and wide distribution of low Schottky barrier height (SBH) patches at Au/n-Si interface, and particular distribution of N_{ss} at Si/TiO_2 interface [27,30–32].

The series resistance (R_s) and shunt resistance (R_{sh}) are determined from the structure resistance (R_i) versus applied bias voltage (V_i) plot determined from the I–V characteristics where $R_i = dV_i/dI_i$ and they were given in Fig. 2. It was observed that at sufficiently high forward bias voltage the structure's resistance values approach to a constant value such that the series resistance (R_s) values for Au/n-Si structures with anatase and rutile phase TiO_2 were found as 209 Ω and 59 Ω, respectively. Similarly, also at sufficiently high reverse bias voltage, the structure resistance values have a constant value, which is equal to structure's shunt resistance (R_{sh}), such that they are 42 kΩ and 598 kΩ for Au/n-Si structures with anatase and rutile phase TiO_2, respectively.

There is a decrease in R_s and an increase in R_{sh} with the increasing annealing temperature. Such behavior of R_s and R_{sh} is a strong evidence of structural improvement with the increasing annealing temperature. In addition, the value of R_s was calculated from the forward bias I–V data using the method of Cheung and Cheung [44]. From Eq. (1), the following functions can be rewritten as:

$$\frac{dV}{d(\ln I)} = n\left(\frac{kT}{q}\right) + IR_s \tag{4a}$$

$$H(I) = V + n\frac{kT}{q}\ln\left(\frac{I}{AA^*T^2}\right) = n\Phi_{Bo} + IR_s \tag{4b}$$

Here, in Eq. (4a) the term IR_s is the voltage drop across the series resistance of the Au/TiO_2/n-Si structures. The $dV/d(\ln I) - I$ and $H(I) - I$ plots of the structures were given in Figs. 3 and 4, respectively. In $dV/d(\ln I) - I$ plot, the plot's slope gives the R_s value, while the y-axis intercept gives the n value. According to Fig. 3, the R_s and n values for Au/n-Si structures with anatase and rutile phases TiO_2 interfacial layer was found as 192.3 Ω and 48.5 Ω, and 8.9 and 6.1.

In $H(I) - I$ graph given in Fig. 4, the plot's slope gives the R_s value as the slope of $dV/d(\ln I) - I$ plot. In addition, using the n value extracted from ln I–V plot and the y-axis intercept, one can find the Φ_{Bo} value. According to Fig. 4, the R_s and Φ_{Bo} values for Au/n-Si structures with anatase and rutile phase TiO_2 interfacial layer was found as 205.2 Ω, 46.0 Ω and 0.653 eV, 0.671 eV. The R_s values obtained from $dV/d(\ln I) - I$ and $H(I) - I$ plots are in a good agreement with each other and the values obtained from ln I–V graph.

To understand the current conduction mechanism in detail or to understand the deviation of ln I–V plots from the linearity at the forward bias, the double logarithmic $\log(I) - \log(V)$ plot can be used in addition to ln I–V plot as given in Fig. 5.

According to the Fig. 5, both of plots have three distinct linear regions (region 1: $-3\,V < V < -1.4\,V$; region 2: $-1\,V < V < -0.6\,V$; region 3: $0.2\,V < V < 2\,V$) that obey $I \alpha V^m$ change. Here, m represents the slope of the each regions' linear section and was found as 1.60, 4.35 and 1.73 for Au/n-Si structure with anatase phase TiO_2 and 1.89, 11.70 and 2.02 for Au/n-Si structure with rutile phase TiO_2, respectively. At low bias region (region 1), the current conduction mechanism for both of the samples exhibits an ohmic behavior, that is, the current is directly proportional to applied bias voltage [45]. This behavior can be attributed to the superiority of bulk-generated current in the film to the injected free carrier generated

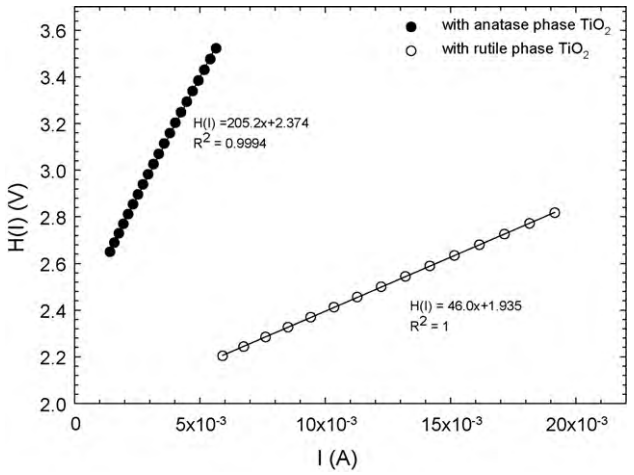

Fig. 4. The $H(I) - I$ characteristics of the Au/n-Si structures with anatase and rutile phase TiO_2 interfacial insulator layer.

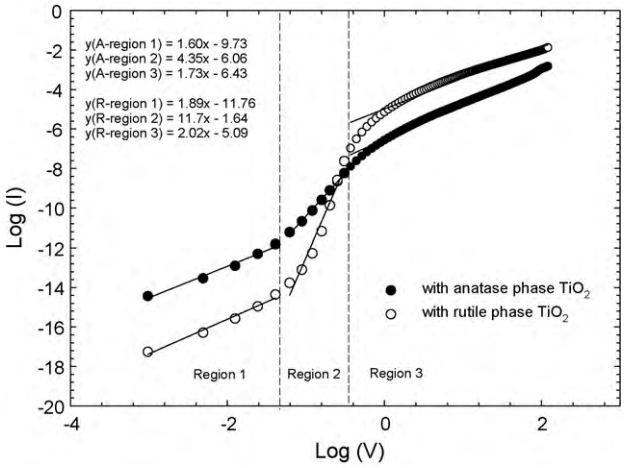

Fig. 5. The $\log(I) - \log(V)$ characteristics of the Au/n-Si structures with anatase and rutile phase TiO_2 interfacial insulator layer.

current [45–47]. The second region for the both samples can be characterized by power law dependence. These behaviors obey the space-charge-limited-current (SCLC) theory that explains the increase in the injected electrons from the electrode to the films with the increasing applied voltage. The increase in the number of injected electrons causes filling up the traps and coming up the space charges [45–47]. At strong forward bias region (region 3), because of the strong electron injection, the electrons escape from the traps and contribute to space-charge-limited-current [45–49].

The non-linearity of $\ln I$–V characteristics at high bias values indicates a continuum of interface states in equilibrium with semiconductor [3]. Thus, the density distribution of the interface states N_{ss} can be determined from the forward bias I–V characteristics. The effective barrier height Φ_e is given as:

$$\Phi_e = \Phi_{Bo} + \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \tag{5}$$

by considering the applied voltage dependency of Φ_e due to the presence of an interfacial insulator layer (TiO_2) and interface states located at the n-Si/TiO_2 interface. For Au/n-Si structures with anatase and rutile phase TiO_2 interfacial insulator layer density of interface states proposed by Card and Rhoderick can be simplified and given as [27]:

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right] \tag{6}$$

where permittivity of semiconductor $\varepsilon_s = 11.8\varepsilon_o$, permittivity of insulator layer $\varepsilon_i = 48\varepsilon_o$ for anatase phase and $\varepsilon_i = 89\varepsilon_o$ for rutile phase TiO_2 [1] while ε_o ($=8.85 \times 10^{-14}$ F/cm) is the permittivity of free space and W_D is the width of the space-charge region.

The capacitance–voltage (C–V) measurements were performed at 1 MHz frequency for the Au/n-Si structures with anatase and rutile phase TiO_2 interfacial insulator layer in order to find the interfacial insulator layer thickness δ using the equation for insulator layer capacitance ($C_{ox} = \varepsilon_i\varepsilon_o A/\delta$) and the other electrical parameters such as built-in voltage V_i, Fermi energy E_F, donor concentration N_d and the width of the space-charge region W_D. At this sufficiently high frequency (1 MHz), the N_{ss} cannot follow the ac signal and the contribution of interface states' capacitance to the total capacitance may be neglected. The thicknesses of the anatase and rutile phase TiO_2 interfacial insulator layers were calculated as 1516 Å, 2120 Å, respectively. The interfacial insulator layers thickness increased with increasing temperature due to the formation of SiO_2 insulator layer at the TiO_2/n-Si interface [26]. The C–V and C^{-2}–V characteristics of the structures were given in Fig. 6. As it can be seen from Fig. 6, the C^{-2}–V plot of the Au/n-Si structures with anatase and

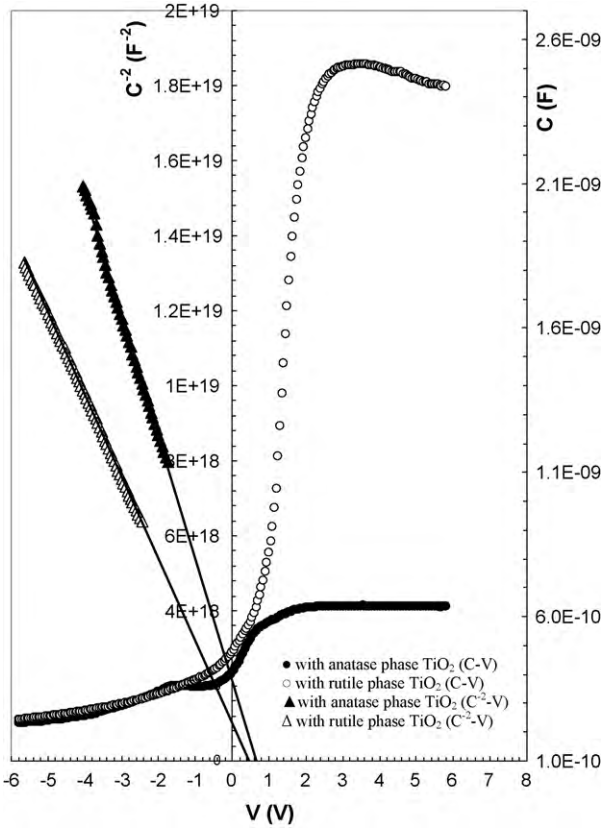

Fig. 6. The C–V and C^{-2}–V plots of Au/n-Si structures with anatase and rutile phase TiO_2 interfacial insulator layer.

rutile phase TiO_2 interfacial insulator layer give a straight line in wide range of bias voltage.

The depletion layer capacitance is given as [50].

$$C^{-2} = \frac{2(V_R + V_i)}{q\varepsilon_s N_d A^2} \tag{7}$$

where V_R is the reverse bias voltage, N_d is the doping concentration and V_i is the built-in voltage at zero-bias, and it can be obtained by means of extrapolation of the C^{-2}–V plot to the voltage axis as 0.667 V and 0.500 V for the structures with anatase and rutile phases TiO_2 respectively. In addition, the doping concentration for the both structures was calculated as 1.87×10^{17} cm^{-3}. Using the obtained V_i values the diffusion potential values at zero-bias were calculated using the following relation

$$V_d = V_i + \frac{kT}{q} \tag{8}$$

and they were found as 0.692 V and 0.525 V for the anatase and rutile phases TiO_2, respectively. The depletion layer width W_D values for both samples were also calculated from C^{-2}–V plots at 1 MHz frequency using the following equation [29]

$$W_D = \sqrt{\frac{2\varepsilon_s\varepsilon_o V_d}{qN_d}} \tag{9}$$

and they were found as 140 Å and 122 Å for the Au/n-Si structures with anatase and rutile phases TiO_2, respectively.

The Fermi energy level expression can be given as

$$E_F = \frac{kT}{q} Ln\left(\frac{N_c}{N_d}\right) \tag{10}$$

where N_c is the effective density of states in the Si conductance band and given as 2.86×10^{19} cm^{-3} [29]. The Fermi energy levels

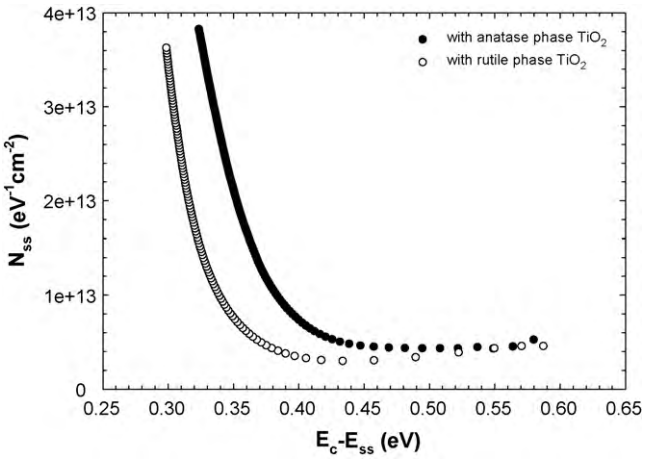

Fig. 7. Density of interface states as a function of $E_c - E_{ss}$ of Au/n-Si structures with anatase and rutile phase TiO_2 interfacial insulator layer.

for both structures were calculated as 128 meV.

Thus, barrier height for the structures was obtained from *C–V* characteristics using the following relation neglecting the image force barrier lowering ($\Delta\Phi_B$)

$$\Phi_B(C-V) = V_d + E_F \tag{11}$$

and they were found as 0.820 eV and 0.753 eV for the Au/n-Si structures with anatase and rutile phases TiO_2 respectively. These obtained values are in a good agreement with the barrier height values obtained from *I–V* characteristics and Cheung functions.

Furthermore, in n-type semiconductors, the energy of the interface states E_{ss} with respect to the bottom of the conduction band at the surface of semiconductor is given by:

$$E_c - E_{ss} = q(\Phi_e - V) \tag{12}$$

The density of interface states N_{ss}, as a function of $E_c - E_{ss}$, of Au/n-Si structures with anatase and rutile phase TiO_2 interfacial insulator layer was given in Fig. 7. As shown in Fig. 7, decrease in N_{ss} from mid gap towards the bottom of conduction band with the increasing annealing temperature is very clear. The magnitude of the N_{ss} of Au/n-Si structure with rutile phase TiO_2 is three times lower than that of anatase phase TiO_2. This behavior was attributed to the molecular restructuring and reordering of Si and TiO_2 molecules at the metal–semiconductor interface [51], the particular distribution of N_{ss} in the semiconductor band gap [52–54] and the better passivation property of rutile phase TiO_2 compared to anatase phase TiO_2 as a result of annealing temperature.

4. Conclusions

The main electrical parameters of Au/n-Si structures with anatase and rutile phase TiO_2 interfacial insulator layer were investigated using *I–V* and *C–V* measurement methods at room temperature and compared with each other in terms of the effect of annealing temperature. The HRXRD patterns showed that the phase transition from amorphous phase to anatase and rutile phases occurs at 700 °C and 900 °C, respectively. Experimental results show that annealing temperature strongly affects the main electrical parameters, such as n, Φ_B, R_s, R_{sh} and N_{ss}. The rectifying ratio of Au/n-Si structure with rutile phase was found as 63 times higher than that of anatase phase TiO_2. Similarly, the leakage current of rutile phase was found to be 15 times lower than that of anatase phase. The energy distribution profile of N_{ss} at TiO_2/n-Si interface of the structures were extracted from the forward bias *I–V* data by taking the bias dependence of Φ_e into account and the N_{ss} values of both structures increase from the midgap towards the bottom of conduction band and decrease considerably with the increasing annealing temperature. In addition, the values of R_s and R_{sh} were found to be as 209 Ω and 42 kΩ for the anatase phase TiO_2 and 59 Ω and 598 kΩ for the rutile phase TiO_2. As a result, the Au/n-Si structures with rutile phase TiO_2 interfacial insulator layer showed better device performance and was found to be more suitable for this type of device fabrications.

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